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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,857	06/25/2001	Huck Khim Koay	70990051-3	1972

7590 11/06/2002

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EXAMINER
SOWARD, IDA M

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,857	KOAY ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the amendment filed August 9, 2002.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (6,069,440) in view of Lester et al. (5,777,433).

Shimizu et al. discloses a light emitting diode comprises of light emitting component capable of emitting light of high luminance with light emitting characteristic which is stable over a long time of use, thus providing a LED capable which experiences only extremely low degrees of deterioration in emission light intensity, light emission efficiency and color shift over a long time of use with high luminance.

Regarding claim 1 (parts a-e), Shimizu et al. disclose a chip type light emitting diode, wherein light emitting diode (LED chip) 202 is installed in a recess of a casing 204 with tapering wall which is filled with a coating material which contains a specified phosphor to form a coating. (Fig. 1-2)(Col. 8, lines 55-67) The conductive wires 103, 203 should have good electric conductivity, good thermal conductivity and good mechanical connection with the electrodes of the light emitting components 102, 202.

The conductive wire may be metal such as gold, copper, platinum and aluminum or an alloy thereof. The light-emitting components 202 are connected to metal terminal 205 installed on the casing 204 by means of conductive wires 203. (Figs. 1-2)(Col. 9, lines 15-36)(Col. 8, lines 55-67) The coating material may be a transparent material having good weatherability such as epoxy resin, urea resin and silicone or glass. (Figs. 1-2)(Col. 16, lines 43-57)

It is evident that Shimizu et al. anticipate claim 1 by disclosing that the LED is mounted on the recess casing, the conductive wire may be a metal and connected to the electrode of the LED, transparent material serves as coating.

Regarding claim 2, Shimizu et al. disclose a chip type light emitting diode, wherein light emitting diode (LED chip) 202 is installed in a recess of a casing 204 with tapering wall where light is extracted from the substrate side and is configured for mounting the electrodes to oppose the cup 105a) is used, Ag paste, carbon paste, metallic bump or the like can be used for bonding and electrically connecting the light emitting component and the mount lead at the same time. Further, in order to improve the efficiency of light utilization of the light emitting diode, surface of the cup of the mount lead whereon the light-emitting component is mounted may be mirror-polished to give reflecting function to the surface, (Figs. 1-2)(Col. 15, lines 55-67)(Col. 16, lines 1-15).

Regarding claim 3, Shimizu et al. disclose a chip type light emitting diode, wherein light emitting diode (LED chip) 202 is installed in a recess of a casing 204 with tapering wall where metallic layer form the terminal interconnects 103, 203. The

conductive wire may be a metal such as gold, copper, platinum and aluminum or an alloy thereof (Figs. 1-2)(Col. 15, lines 15-36)

Regarding claim 5, Shimizu et al. disclose a chip type light emitting diode, wherein light emitting diode (LED chip) 202 is installed in a recess of a casing 204 with tapering wall where metallic layer form the terminal interconnects 103, 203. The light emitting components 202 are connected to exposed metal terminals 205 installed on the casing 204 by means of conductive wires 203. Good connectivity with the bonding wires which are conductive wires and good electrical conductivity are required. Specifically, the electric resistance is preferably within 300 .mu.Ω-cm and more preferably within 3 .mu. Ω-cm. (Figs. 1-2)(Col. 16, lines 55-67)(Col. 16, lines 1-15) Materials which satisfy these requirements contain iron, copper, iron-containing copper, tin-containing copper, copper-, gold- or silver-plated aluminum, iron and copper. (Figs. 1-2)(Col. 16, lines 35-42)

However, Shimizu et al. fail to disclose a planar substrate; first and second interconnects between upper and lower surfaces of the substrate; transparent encapsulant material; and connecting the chip type LED to a terminal using a metallic layer.

Lester et al. disclose a planar substrate; first 43 and second 45 interconnects between upper and lower surfaces of the substrate; transparent encapsulant material 41 bonded to the substrate; and connecting the chip type LED 42 to a terminal using a metallic layer 25 (Figures 1-2, col. cols. 1 and 4, lines 15-41 and 10-20, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LED structure of Shimizu et al. with the transparent encapsulated chip type LED of Lester et al. to improve the efficiency of the light emitting device.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (6,069,440) and Lester et al. (5,777,433) as applied to claims 1, 3 and 5 above, and further in view of Okazaki et al. (5,298,768).

Shimizu et al. and Lester et al. disclose all mentioned in the rejection above. However, Shimizu et al. and Lester et al. fail to disclose the side wall of the recess is plated with a metallic layer. Okazaki et al. disclose side wall of the recess is plated with a metallic layer 7 & 8 (Figure 6, col. 4, lines 21-64). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the LED structure of Shimizu et al. and the transparent encapsulated chip type LED of Lester et al. with the metallic plated side walls of Okazaki et al. to reduce manufacturing costs.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu et al. (6,069,440) and Lester et al. (5,777,433) as applied to claims 1, 3 and 5 above, and further in view of Hochstein (6,045,240).

Shimizu et al. and Lester et al. disclose all mentioned in the rejection above. However, Shimizu et al. and Lester et al. fail to disclose first and second vias extending

between the upper surfaces of the substrate. Regarding claim 4, Shimizu et al. disclose a light emitting diode comprises of light emitting light of high luminance with light emitting characteristic which is stable over a long time of use, thus providing a LED capable which experiences only extremely low degrees of deterioration in emission light intensity, light emission efficiency and color shift over a long time of use with high luminance. (Figs. 1-2)(Col. 8, lines 55-67)

However, Shimizu et al. are silent on how to assemble multiple of such light emitting diodes on an electrically driven L.E.D. lamp assembly comprising an electrically insulating circuit board substrate having opposed first and second surfaces with vias or holes separation.

Regarding claim 4, Hochstein describes how to made an electrically driven L.E.D. lamp assembly (14) comprising an electrically insulating circuit board or substrate 26 having opposed first and second surfaces. (Abstract) a plurality of holes extend through the board 26 and plurality of pads 50 of thermally conductive plating are disposed on the second side with each pad 50 associated with the leads to conduct heat from each of the leads to one of the pads 50 while maintaining electrical isolation between the pads. In some instances the holes may be holes through which LED leads 30 and 32 extend with each of the lead holes providing thermal conductivity to one of the pads 50. In addition to the lead holes for the leads 30 and 32, there may be included a plurality of holes 52 dispersed among the lead holes. (Fig. 5)(Col. 5, lines 31-55). Hochstein further discloses an ellipsoidal done having a major axis equal to the

length of the planar substrate and a minor axis equal to the width of the substrate (Figure 3).

Therefore, modifying the LED structure of Shimizu et al. and the transparent encapsulated chip type LED of Lester et al. with the vias of Hochstein is the evidence that it would have been obvious for one of ordinary skill in the art at the time the invention was made to have recognized to use holes or vias isolation to separate the multiple LED in a same substrate.

Response to Arguments

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to light sources:

Ishinaga (US 6,355,946 B1)

Lowery (5,959,316)

Wojnarowski et al. ((US 6,407,411 B1).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
November 3, 2002

Stephen D. Meier
Primary Examiner